CLAIMS

1. Integrated circuitry comprising:

a monolithic semiconductive substrate;

a power semiconductor switching device comprising a plurality of field effect transistors formed using the monolithic semiconductive substrate and having a plurality of electrical contacts including a plurality of gate contacts, a plurality of source contacts coupled in parallel and a plurality of drain contacts coupled in parallel; and

auxiliary circuitry formed using the monolithic semiconductive substrate and configured to couple with at least one of the electrical contacts of the power field effect transistors.

2. The circuitry of claim 1 wherein the field effect transistors comprise planar field effect transistors.

3. The circuitry of claim 1 wherein the auxiliary circuitry comprises a gate driver amplifier configured to provide a control signal to the electrical contacts of the field effect transistors comprising the gate contacts.

4. The circuitry of claim 1 wherein the auxiliary circuitry comprises a power converter controller configured to provide a control signal to the electrical contacts of the field effect transistors comprising the gate contacts.

5. The circuitry of claim 1 wherein the gate contacts are coupled in parallel.

6. The circuitry of claim 1 wherein the auxiliary circuitry comprises an application specific integrated circuit.

7. The circuitry of claim 1 wherein the auxiliary circuitry comprises a zero-current switching/timing circuit.

8. The circuitry of claim 1 wherein the auxiliary circuitry comprises a load protection circuit.

9. The circuitry of claim 1 wherein the auxiliary circuitry comprises an active snubber circuit.

10. The circuitry of claim 1 wherein the power semiconductor switching device and the auxiliary circuitry are formed upon a die.

11. The circuitry of claim 1 wherein the field effect transistors comprise MOSFET devices.

12. A method of forming a power transistor comprising:

providing a monolithic semiconductive substrate having a surface;

forming a power field effect transistor using the monolithic substrate and having a source contact and a drain contact adjacent to the surface; and

forming auxiliary circuitry using the monolithic semiconductive substrate, the forming comprising coupling the auxiliary circuitry with at least one contact of the power field effect transistor.

13. The method of claim 12 wherein providing comprises providing the substrate comprising a semiconductor die.

14. The method of claim 12 wherein the forming the power field effect transistor comprises forming a plurality of planar field effect transistors electrically coupled in parallel.

15. The method of claim 12 wherein the forming auxiliary circuitry comprises forming a gate driver amplifier configured to provide a control signal to a gate contact of the power field effect transistor.

16. The method of claim 12 wherein the forming auxiliary circuitry comprises forming a power converter controller configured to provide a control signal to a gate contact of the power field effect transistor.

17. The method of claim 12 wherein the forming auxiliary circuitry comprises forming the auxiliary circuitry comprising application specific integrated circuitry.

18. The method of claim 12 wherein the formings individually comprise forming the power field effect transistor and the auxiliary circuitry comprising CMOS devices.

19. The method of claim 12 wherein the forming auxiliary circuitry comprises forming the auxiliary circuitry comprising zero-current switching\timing circuitry.

20. The method of claim 12 wherein the forming auxiliary circuitry comprises forming the auxiliary circuitry comprising active snubber circuitry.

21. The method of claim 12 wherein the forming auxiliary circuitry comprises forming the auxiliary circuitry comprising load protection circuitry.

22. The method of claim 12 wherein the forming the power field effect transistor comprises forming a plurality of MOSFET devices.